Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A manufacturing method of a flash memory, comprising:

forming a patterned first dielectric layer, a patterned first conductive layer and a patterned hard mask layer on a substrate;

forming a conformal second conductive layer over the substrate;

etching back the second conductive layer by using the hard mask layer as a etching stop layer for forming a conductive spacer on both sidewalls of the first conductive layer;

removing the hard mask layer;

forming a second dielectric layer and a third conductive layer over the substrate;

constructing a stacked gate structure having the third conductive layer, the second dielectric layer, the first conductive layer, the conductive spacer and the first dielectric layer;

wherein a floating gate of the stacked gate structure is constructed by a remainder portion of the first conductive layer and the conductive spacer; and

forming a source/drain region on both sides of the s

stacked gate structure within the substrate.

[c2] 2. The manufacturing method of a flash memory of claim 1, wherein the step of forming the patterned first dielectric layer, the patterned first conductive layer and the patterned hard mask layer comprises;
forming a third dielectric layer, a fourth conductive layer and a hard mask material layer on the substrate; and
patterning the third dielectric layer, the fourth conductive layer and the hard mask material layer to form the patterned first dielectric layer, the patterned first conductive layer and the patterned hard mask layer on the substrate.

[c3] 3. The manufacturing method of a flash memory of claim 1, wherein a material of the hard mask layer is one selected from a group consisting of a silicon nitride, a silicon oxynitride, a silicon oxide or a spin on glass (SOG).

[c4] 4. The manufacturing method of a flash memory of claim 1, wherein the step of forming the hard mask layer comprises a chemical vapor deposition (CVD) or a spin coating method.

[c5] 5. The manufacturing method of a flash memory of claim 1, wherein a thickness of the hard mask layer is in a range of about 0.1 nm to about 20 nm.

[c6] 6. The manufacturing method of a flash memory of claim 1, wherein a material of the first conductive layer comprises a doped polysilicon.

[c7] 7. The manufacturing method of a flash memory of claim 1, wherein a material of the conformal second conductive layer comprises a doped polysilicon.

[c8] 8. The manufacturing method of a flash memory of claim 1, wherein the step of forming the conformal second conductive layer comprises a chemical vapor deposition (CVD) method.

[c9] 9. The manufacturing method of a flash memory of claim 1, wherein a thickness of the conformal second conductive layer is in a range of about 0.1 nm to about 100 nm.

[c10] 10. A structure of a flash memory, comprising:
a substrate ;
a floating gate disposed on the substrate, wherein the floating gate comprises:
a patterned conductive layer disposed on the substrate; and
a conductive spacer disposed on both sidewalls of the patterned conductive layer;
a tunnel oxide layer disposed between the substrate and the floating gate;

a control gate disposed on the floating gate;
an inter-poly dielectric disposed between the control gate and the floating gate, wherein a stacked gate structure is constructed by the tunnel oxide layer, the floating gate, the inter-poly dielectric and the control gate; and
a source region and a drain region, disposed in both side of the stacked gate structure within the substrate.

[c11] 11. The structure of a flash memory of claim 10, wherein a material of the conductive layer comprises a doped polysilicon.

[c12] 12. The structure of a flash memory of claim 10, wherein a material of the conductive spacer comprises a doped polysilicon.

[c13] 13. The structure of a flash memory of claim 10, wherein the source region and the drain region are disposed in both side of the conductive layer without the conductive spacer.